Trap-Free Process and Thermal Limitations on Large-Periphery SiC MESFET for RF and Microwave Power

Frédéric Villard, J.-P. Prigent, E. Morvan, C. Dua, C. Brylinski, F. Temcamani, and P. Pouvil, *Member, IEEE*

***Abstract*—In this paper, we present recent results on an SiC MESFET and we describe two of the main limitation mechanisms encountered: the self-heating and the trapping effects. Results on recent MESFET devices processed by THALES Research and Technology (TRT), Colombes, France, show that the trapping effects has been solved by using epitaxial layers on a higher purity 4H-SiC semi-insulating substrate sample made with a new technique by Okmetic, Vantaa, Finland. The association of two chips in the same case showed that the main limitation mechanism for power density originates from self-heating effects, which could be solved by optimizing the chip layout. 37.8-W output power at 500 MHz, 1.78-W/mm power density, and 35-dB third-order intermodulation-distortion ratio are the best obtained performances. An experimental analysis of trapping and self-heating effects on large-periphery SiC MESFETs is proposed in this paper.**

***Index Terms*—MESFET, self-heating, silicon carbide (SiC), trapping.**

I. Introduction

SILICON carbide (SiC) is a wide-bandgap material that has great potentialities for power amplification in the radio-communication area [high-density television (HDTV), and global system for mobile communication (GSM) second generation (2G) and third generation (3G)] [1]–[4]. Over 200 crystal varieties, which are different by their atomic arrangement, are known. Current researches involves the polytypes 3C, 6H, and mainly the 4H [5] for RF and microwave power MESFET transistors [1]–[13].

The main physical properties of 4H-SiC [5], [6] are a wide bandgap (3.26 eV, three times more than silicon) and a high thermal conductivity (twice or triple that of silicon). This allows operation at higher temperature and easier cooling of the chip. The breakdown field, ten times greater than in silicon, allows to operate devices at a high supply voltage. The saturation velocity is twice greater than in silicon, which leads to a high saturation current. Low electronic mobility is the main drawback of SiC. It increases the channel resistance and, consequently, the knee voltage (typically 10–15 V in our transistors designed for 0.3-A/mm I_{DSS} and 200-V breakdown voltage). This problem is compensated by the MESFET high operating drain bias voltage (over 70 V demonstrated) [4], [6].

The SiC advantages have direct consequences on power-amplifier design [3], [4]. For example, the high drain voltage enables to obtain output impedance close to 50 Ω and, thus, simplifies the broad-band matching, increases the band periphery, decreases the losses in the matching circuits, and finally reduces the amplifier's cost. The high power-density capability simplifies the amplification systems by reducing the number of elementary cells in parallel.

II. Recent Performances and Analysis of SiC Large-Periphery Mesfet Limitations

Recent literature on SiC MESFETs confirmed these potentialities. Some examples are as follows:

- 45-W continuous wave (CW) in class A–B with a single chip of 31.5 mm ($f = 1.5$ GHz, $V_{\mathrm{DS}} = 55$ V, power-added efficiency (PAE) 51%) [4];
- 80-W CW with a 48-mm-width MESFET, which corresponds to 1.7 W/mm ($f = 3.1$ GHz at $V_{\mathrm{DS}} = 40$ or 50 V) [13];
- 4.3-W/mm power density (1.1-W output power) and 9-dB gain at 10 GHz [13];
- 5.2-W/mm power density (1.3-W output power) and 63% PAE at 3.5 GHz [2].

However, although these performances were very promising, two limitations have appeared, i.e., the self-heating and trapping effects.

A. Self-Heating Effects

The majority of published papers are related to small-gate-periphery MESFETs [2], [7], [8], [13]. In these conditions, thermal problems are limited and the power densities show records (up to more than 5 W/mm [2]). Specific studies demonstrated SiC MESFET self-heating phenomena even for peripheries lower than 1 mm [14], [15] in spite of good thermal conductivity of SiC. When the gate periphery increases, the power densities decrease very quickly (measurement results are presented in Table I). The reason for this is related to the self-heating effect. For a wide transistor, the temperature becomes very high and,

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F. Villard, F. Temcamani, and P. Pouvil are with the Department of Radio CIME, Ecole Nationale Superieure de l'Electronique et de ses Applications–Electronic, Communication and Micro-Wave Laboratory, 95014 Cergy-Pontoise, France (e-mail: frederic.villard@fr.thalesgroup.com; temcamani@ensea.fr; pouvil@ensea.fr).

J.-P. Prigent is with THALES Communications France, BP82 Colombes 92704, France (e-mail: jean-paul.prigent@fr.thalesgroup.com).

E. Morvan, C. Dua, and C. Brylinski are with the THALES Research and Technology Laboratory, Domaine de Corbeville, 91404 Orsay Cedex, France.

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TABLE I
DRAIN CURRENT DENSITY DRAIN WITH $V_{DS} = 10$ V AND $V_{GS} = 0$ V

Gate periphery	Drain current Idss (A)	Drain current Density (mA/mm)
10.8 mm	1.9	176
21.6 mm	2.2	103
31.5mm	3.3	106
36mm	3.2	88

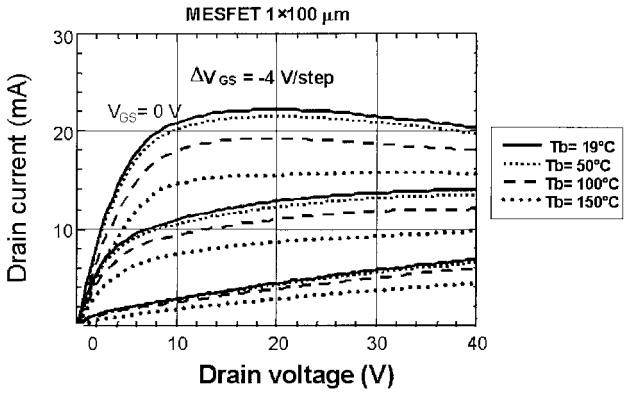
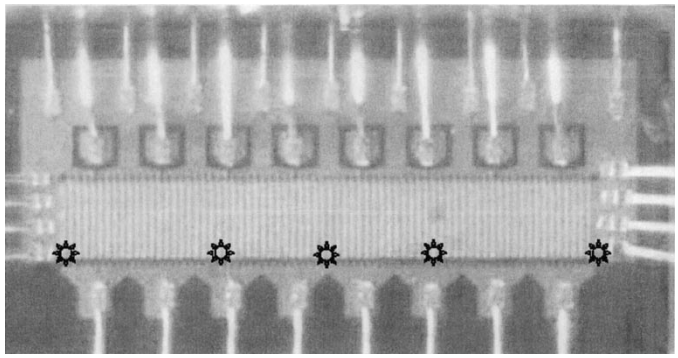
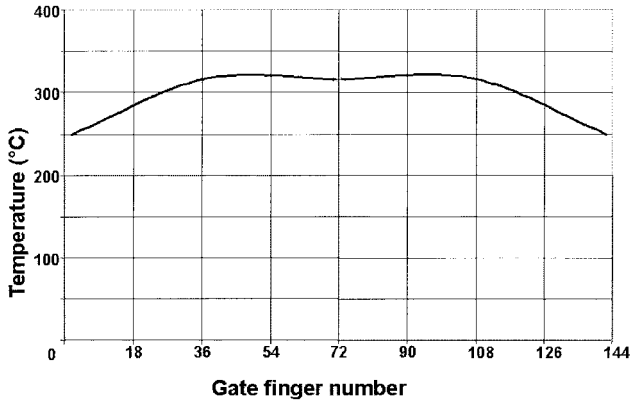


Fig. 1. Influence of the case temperature on the I–V characteristics.



(a)



(b)

Fig. 2. Temperature profile on a wide SiC MESFET: 144 gate fingers, 250-μm finger periphery, 36-mm total gate periphery, 58.6 W (1.63 W/mm) of dissipated power. Measurement points are indicated by asterisks.

therefore, the electronic mobility decreases [14], together with the drain current, and finally, the RF power goes down.

To demonstrate the correlation of decreasing performances with the component self-heating, we have performed two kinds of measurements. In the first one, we artificially increased the channel temperature of a 100-μm-periphery MESFET by increasing the heat-sink temperature (noted as Tb) to show the effect on the I–V curve. The transistor (with a 400-μm SiC substrate) was brazed on a case, which was mounted on the heat sink. Fig. 1 shows the I–V characteristics for various Tb values, from 19 °C up to 150 °C. The corresponding channel temperature $T_{\rm ch}$ was estimated by a thermal simplified model

$$T_{\rm ch} = T_b + R_{\rm th} \cdot P. \tag{1}$$

$T_{\rm ch}$, T_b, $R_{\rm th}$, and P are the channel temperature, heat-sink temperature, thermal resistance, and dissipated power, respectively. The thermal resistance includes the active device (several fingers with variable width), stacked elements (braze, case, and SiC substrate), and a pyramidal propagation of heat.

Calculations give $T_{\rm ch}$ values varying from 65 °C to 230 °C for the various design configurations. The related decrease of the drain current is approximately 30%. In these conditions, the RF available power density decreases at least in the same ratio. This first set of measurements allows to highlights the effect of the temperature on a MESFET transistor. The estimate of the thermal resistance can be refined by taking into account the expected variation of electron mobility.

In the second kind of measurements, we have applied Raman spectrometry to evaluate the channel temperature on large transistors (10.8–36-mm periphery). Raman spectrometry consists in exciting the crystal atoms by a laser beam, and measuring the Stokes and anti-Stokes rays of light nonelastically diffused by the lattice vibrations. The depth extension of temperature probing zone is approximately 1 μm. The heat-sink temperature was maintained at 20 °C and the device was only dc biased without any RF excitation. The dissipated power was 58.6 W. This power is an estimation of the MESFET dissipation in class A–B. Fig. 2 shows the result of measurement for a 36-mm device. The curve on right-hand side shows the channel temperature profile. 328 °C was measured near the center of the chip. To confirm these values, the temperature was calculated using the (1). We suppose a uniform profile for $T_{\rm ch}$ and a nonlinear behavior of the thermal resistance following [14]. In Table II, we have compared the measured and calculated temperatures for four different values of gate peripheries at the same power density. Experiment and simulation are in good agreement and show a very high temperature of the MESFET channel, much over the optimum temperature.

In conclusion, due to the high power density, careful thermal management of the SiC MESFET is necessary (as for any other power device). To work out this kind of problem, a thermoelectrical model built by Royet *et al.* [14] can be used as a useful tool to optimize the transistor geometry. Such a model is now under development.

TABLE II
MEASURED AND CALCULATED CHANNEL TEMPERATURES

MESFET Width	Measured	Simulated Thermal Model
10.8 mm	134°C	160°C
21.6 mm	265°C	275°C
31.5mm	340°C	350°C
36mm	337°C	346°C

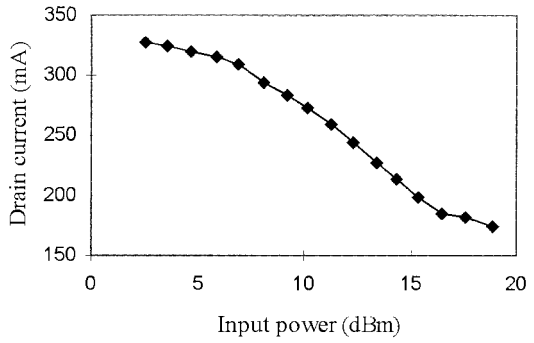


Fig. 3. Drain current decreases under RF operation due to the trapping effect.

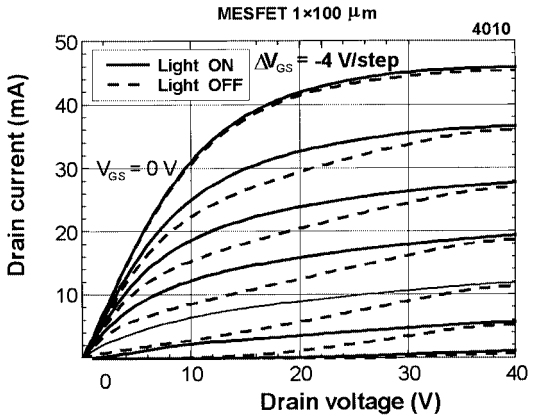


Fig. 4. Influence of light on the I–V characteristics.

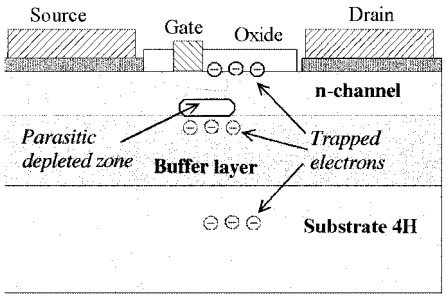


Fig. 5. Trapped electrons in SiC MESFET.

B. Trapping Effects

The second limitation observed in all our SiC MESFET devices until recently has been related to trapping effects. Several phenomena were observed. In static measurements, we have observed a spontaneous drain-current drift. This drift is generally characterized by a reduction, and occasionally by hopping behavior, of the drain current. The current decrease rate strongly depends on the substrate and epitaxy type. Under RF operation, the trapping phenomenon is different. One major phenomenon is the reduction of the dc drain current as the input RF power is increased (Fig. 3). This decrease happens in place of the normal drain-current expansion in class-A–B operation. This phenomenon is very deleterious to RF performance because it decreases the transistor available power and destroys device linearity.

Many recent studies were carried out to analyze and reduce trapping effects. To easily evidence the presence of traps, I–V characteristics were measured without light and then with light (Fig. 4), respectively. When the light is turned off, the current experiences severe decrease, and we get the kind of I–V characteristics denoted by the dotted line. When the light is turned on, we recover the initial characteristics (denoted by the continuous line). This behavior is classically related to the trapping of electrons (for instance, like for AsGa and GaN devices). To find the traps localization, several assumptions were considered. The final cause we found after a long investigations is the charging of deep levels in the substrate, which contributes to pinchoff of the channel from the bottom by creating a "bottom gate" (back bating, see Fig. 5). The deep levels are a very probable consequence of the substrate compensation by vanadium, which gives the material its semi-insulating properties. This phenomenon can arise in static operation by the injection of electrons into the substrate as a result of the very strong electric-field vertical component. It produces an undesirable accumulation of negative charge near the channel. Siriex *et al.* [16] showed by comparing measured and simulated results that the back gating may also explain the RF trapping phenomenon. A solution was first investigated by trying several sets of values for the buffer thickness and doping level in order to try to insulate the channel from the substrate. However, the buffer option has limitations. The control of this layer must be perfect, otherwise it will itself be the scene of other types of drift phenomena.

The second possible assumption is the presence of traps at the interface between the passivation oxide and channel (surface states). The oxide is deposited on the surface of the MESFET in order to get surface passivation and insulate the electric connections and further bonding. Contamination of this oxide by carbon and aluminum atoms has been reported in the literature, either inside the insulator or at the interface [17], [18]. It could contribute in the same way to pinch off the channel from the top (Fig. 5).

The traps nature and density depend on the surface quality on which the oxide is deposited. We note however that Siriex *et al.* [16] have shown, using pulsed measurements, that the surface states were negligible in tested MESFETs compared to the buffer or substrate traps.

In both assumptions, the ultimate solution to trapping effects seems to reside in the improvement of material quality and growth techniques and not by the artificial use of a buffer, which would mask the trapping effects.

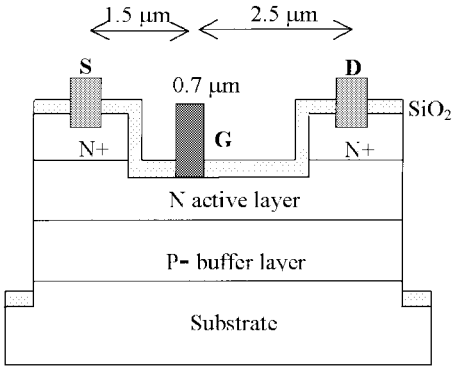


Fig. 6. Cross-sectional view of an SiC MESFET elementary cell.

III. Recent Progress

A MESFET process was carried out by THALES Research and Technology (TRT), Colombes, France, on an epitaxial wafer using a new technique, and supplied by Okmetic, Vantaa, Finland. All MESFETs have a large gate periphery. We present in this paper four gate periphery configurations, i.e., 10.8, 21.6, 31.5, and 36 mm.

A. Technological Considerations—Crystal Purity Issues

Our interpretation of the improvement brought using the Okmetic material is based on the assumption that the traps are a consequence of the vanadium deep centers used, in previous commercial 4H SI substrates, to confer the crystal its semi-insulating properties. Those previous crystals were grown using sublimation technique known as physical vapor transport (PVT). They contained a nitrogen level of approximately $1–2 \times 10^{17}$ cm^{-3}. Even recent "high purity" PVT 4H SI substrates still have a nitrogen level in the mid 10^{16} cm^{-3}. An important margin has to be taken for adapting to nonuniform distribution of both nitrogen and acceptor elements in the crystal. Therefore, for nitrogen residual of approximately $1 \cdot 10^{17}$ cm^{-3}, generally over $3 \cdot 10^{16}$ cm^{-3} deep level centers have to be present in the 4H SI crystals. Each deep level center that is not filled by one electron coming from the nitrogen donors can act as a trap for electrons injected from the active layer of the device. In our samples [3], [4], [10], [11], [14]–[16], Cree PVT substrates were V-doped around mid 10^{16} cm^{-3}, with nitrogen and aluminum levels $1–2 \times 10^{17}$ cm^{-3}, estimated by SIMS. Okmetic HT-CVD [19]–[21] substrates had vanadium content much below 3×10^{15} cm^{-3} and a nitrogen level below the SIMS detection limit (limit around mid 10^{16} cm^{-3}).

For the present process, the substrate thickness is 350–400 μm. The active layer is an n-type with a doping level of 1.6×10^{17} cm^{-3} and a thickness of 0.4 μm . The buffer is typically a p-type with a doping level of $1–5 \times 10^{17}$ cm^{-3} and a thickness in the range of 100–600 nm. The process and layer characteristics are the same as described by Royet *et al.* [14]. (Ohmic contact is carried out by nickel and Schottky contact by Ti/Pt/Au.) The final transistor is a parallel association of elementary cells. A cross view of the elementary cell is presented in Fig. 6.

B. DC Characterization

DC I–V characteristics measurements showed $I_{\rm DSS}$ values summarized in Table II. The explanation of the regular current density decrease with gate periphery (for the same $V_{\rm GS} = 0$ V) is very probably to be found again in transistor self-heating. During measurements, I–V characteristics were stable and no current drift was observed. We conclude on the absence of major dc trapping effects.

C. Power Measurements

CW power measurements were carried out using a load–pull test bench (Focus Microwaves, Quebec, QC, Canada). Frequency was in the range of 500–800 MHz. Drain voltage was limited to 45 V because breakdown voltage of the devices was reduced by problems with air-bridge processing. All output power values were measured at 1-dB compression. The best power density is 1.73 W/mm for a 10.8-mm gate periphery. This is very close to the best result we have obtained yet for such a large gate periphery. Various load–pull measurements in class AB are presented in Table III. $I_{\rm dq}$ represents the bias drain current without RF power and $I_{\rm ds}$ is the average drain current associated with the maximum RF power. We observe an important decrease of the power density with the gate periphery. For example, total output power saturates to very similar values when the gate periphery is increased from 21.6 to 36 mm. It confirms the deleterious of self-heating, already observed for dc measurements.

On the other hand, we did not record any drift of output power with time, even under illumination. It confirms the transistor stability in dc conditions and the absence of active traps. The current increase from $I_{\rm dq}$ to $I_{\rm ds}$ lets us suppose that there are no RF traps either.

The output impedance is equivalent to a 46-Ω resistance in parallel with a 6-pF capacitor. The input impedance is equivalent to a 25–30-Ω resistance in parallel with a 16-pF capacitor. These resistances values are relatively high and the capacitors is low; part of it due to packaging contributions. It makes the SiC MESFET broad-band matching easier [3], [4].

D. Class of Operation

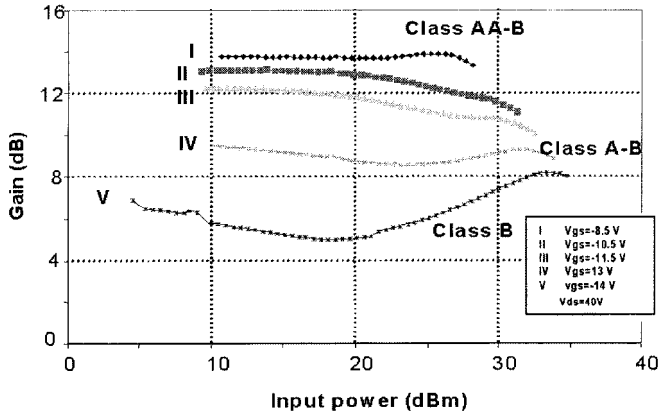
To confirm the traps absence, we have tested the transistors in various operation classes, especially in class B. In this class, the transistor is biased near pinchoff. The current injection in the buffer or in the substrate is maximum and the trapping effects can be activated more easily. Measurements showed (Fig. 7) an expansion of dc drain current $(I_{\rm ds})$ in a ratio of 30 as compared with the quiescent bias current $(I_{\rm dq})$. It is the common behavior of a component without trapping effects. On our previous SiC MESFET devices, we generally observed, even in class-AB operation, an abnormal decrease of the current. The other main results, obtained with a 10.8-mm MESFET in class AA–B, class A–B, and class B, are presented in Table IV and Fig. 7 ($V_{\rm DS} = 40$ V and $f = 500$ MHz).

E. Association of Two Chips

To verify our analysis on the transistor self-heating effects, we have associated two 10.8-mm chips in the same case. It

TABLE III
PERFORMANCE FOR DIFFERENT GATE PERIPHERY

Mesfet Width (mm)	Output Power (W)	Power Gain (dB)	PAE (%)	Frequency (MHz)	Vds (V)	Ids (mA)	Idq (mA)	Vgs (V)	Power Density (W/mm)
10.8	18.7	8	50.3	500	40	779	50	-14	1.73
21.6	24.8	13.1	59.2	500	45	884	300	-13	1.15
31.5	25.7	9.5	52.9	800	40	1078	415	-9.5	0.82
36	25.5	7.5	42.5	800	35	1408	644	-8	0.71



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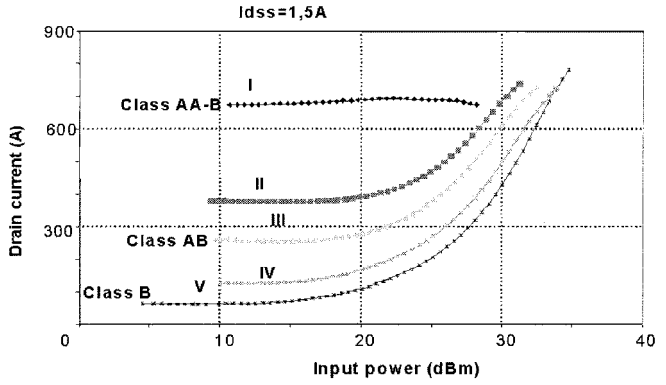

(b)

Fig. 7. Power gain and average drain current of a 10.8-mm MESFET for various operating classes.

TABLE IV
PERFORMANCE OF THE 10.8-mm GATE-PERIPHERY DEVICE OPERATING IN VARIOUS CLASSES

Class	Gain (dB)	Ids (A)	Pout (dBm)	Efficiency (%)
AA-B	13.7	Idss / 2	41.8	55
A-B	10	5 x Idq	42.5	61
B	8	30 x Idq	42.7	60

corresponds to a 21.6-mm total gate periphery. Measurements (Fig. 8) showed the same power density (1.73 W/mm) as for a

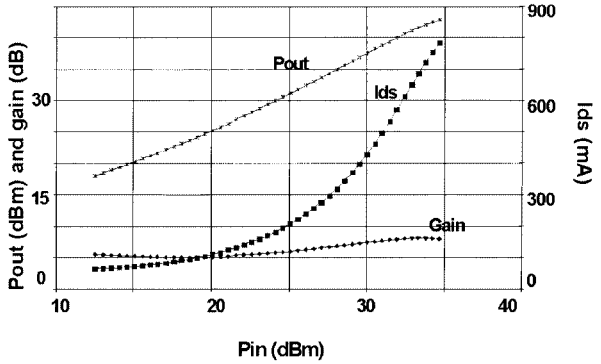

Fig. 8. Class-B performances of the 2×10.8 mm MESFET ($f = 500$ MHz, $V_{DS} = 40$ V).

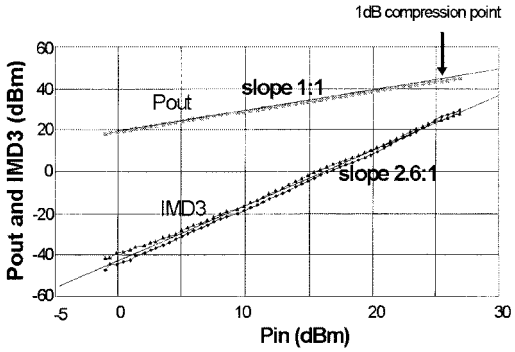

Fig. 9. AM–AM and IMD3 for the 2×10.8 mm MESFET ($V_{ds} = 40$ V, $f = 500$ MHz).

single-chip 10.8-mm transistor. The output power was 37.5 W at 500 MHz. In comparison, we obtained 1.15-W/mm and 24.8-W output power, respectively, for a single-chip 21.6-mm transistor (Table III). The improvement is related to the I_{DSS} current increase, which is almost twice greater for a two-chip device than for a single-chip transistor with the same total periphery. This association confirms our previous studies on the self-heating limitation and means that, in the next SiC MESFET generation, the design must be more spatially diluted to optimize the heat dissipation.

Measurements of third-order intermodulation distortion (IMD3) (Fig. 9) showed a slope close to 3 dB/dB. The IMD3 level with 10-dB backoff from the 1-dB compression point is -35 dB. It should be noted that measurements were performed with 1-MHz frequency offset between tones. With a 10-kHz spacing, the IMD3 ratio was further improved by 3–5 dB.

IV. Conclusion

A theoretical and experimental analysis of trapping and self-heating effects in wide SiC MESFETs has proven the existence of two main limitation factors. The conclusion of a thorough analysis of those two factors has shown that it is necessary to optimize the substrate material purity and the transistor design to get high-power density and stable behavior. As a preliminary result in this way, a new SiC MESFET device has been presented without trapping effects. It was processed by TRT on epitaxial sample supplied from Okmetic on a substrate made using a new crystal growth technique.

DC characteristics and RF power measurements showed very stable behavior, which led us to draw conclusions about the absence of traps. High-power performances were obtained on transistors with large gate periphery (from 10.8 to 36 mm) in spite of a drain voltage handling lower than expected for this device design. We have obtained 18.7-W output power (1.73-W/mm power density) on a MESFET device with 10.8-mm gate periphery. In comparison, a transistor with 36-mm periphery gave only 0.71 W/mm. The latter performance is clearly limited by transistor self-heating. To solve this problem, we have associated two 10.8-mm chips in the same case. We have then obtained the same power density from the double-chip device as for a single-chip 10.8-mm transistor (1.73 W/mm) and we have reached 37.5-W output power. From these results, we are now able to define the geometry of new transistors for optimizing the RF performances: length of the fingers, structure of epitaxy, and quality of the substrate. We have also validated the conclusions of our experimental analysis of the transistor limitations. These new SiC MESFETs can now be used for building true amplifiers, perfectly suitable for building amplifiers, whatever the operating class, which we had never previously obtained. Power, efficiency, and linearity measurement results are very encouraging for the future of this rising technology.

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Frédéric Villard was born in Bourgoin-Jallieu, France, in 1974. He received the Eng. degree in electronics from the National Engineering Scholl of Electronics Application, Ecole Nationale Superieure de l'Electronique et de ses Applications (ENSEA), Cergy-Pontoise, France, in 1999, and is currently working toward the Ph.D. degree at the ENSEA.

In 2000, he joined the SiC team of THALES Communications France, Colombes, France, where he is involved with the building of power amplifiers with SiC MESFETs. He is also involved in linearization techniques and power-amplifier modeling.

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E. Morvan, photograph and biography not available at time of publication.

C. Dua, photograph and biography not available at time of publication.

C. Brylinski, photograph and biography not available at time of publication.

F. Temcamani, photograph and biography not available at time of publication.

P. Pouvil (M'02), photograph and biography not available at time of publication.